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A 1-1/2-Level On-Chip-Decoding Bubble Memory Chip Design

A 1-1/2-level bubble memory on-chip decoder circuit has been designed which can perform the on-chip decoding function and may be fabricated with a gross alignment requirement. This design includes a multiple-channel replicator which can reduce the chip-writing power requirement, a selective annihilating switch which can effectively annihilate bubbles with minimum delay, and a modified transfer switch which can be used as a selective steering-type decoder.

In the bubble memory organization, the on-chip decoding approach has the advantages of lower access time than serial or major/minor loop organization, a small number of control leads, and inherent redundancy capability. For device processing, the single-level circuit approach, with gross aligned conductor pads, simplifies the process procedure and increases the yield. This design presents a 1-1/2-level on-chip decoding circuit which combines the advantages of both approaches.

There are two basic on-chip decoder organizations in the design. In both, the bubbles are separated by a series of generators and are replicated by a set of multiple replicators, so that there is one stream of bubbles propagating toward each storage loop. Before reaching the storage loop, these bubble streams pass a set of selective annihilating switches, which will annihilate every bubble stream except the selected one. In this manner, the information is written into the particular loop selected.

To read out a particular loop, there are two different approaches. For one, the information in all storage loops is replicated simultaneously by a set of replicators. These bubble streams are then selectively annihilated by a set of switches which allows only one selected stream to reach the multiple-input detector. In the other design, the bubble streams pass a set of

steering switches which allows only a selected stream to reach a replicator leading to the multiple-input detector. The rest of the stored information will be steered back to the storage loop before reaching the replicator.

Since the decoder circuit single-level generator, replicator, and multiple-input detector components are already established, only the multiple-channel replicator, the selective annihilating switch, and the selective steering switch will be covered here.

a. Multiple-Channel Replicator — Entered bubbles are expanded by chevron elements and are propagated toward several parallel channels. At the last column of the stretcher area, part of the chevron elements is connected by Permalloy lines through which a current pulse can be passed. This current pulse generates field gradients which split the stripe domain. Thus, a single input can be replicated into several identical outputs. The replicator reduces the number of generators in the circuit and can reduce, also, the required writing power of the chip.

b. Selective Annihilating Switch — The basic annihilator consists of one Permalloy line across the chevron propagation element. If this line is placed at the first half of the chevron, a positive current pulse will only collapse bubbles at that portion of the chevron but not the bubble at the other end. The reverse is true if the Permalloy line is placed at the other half of the chevron, as then a negative current pulse can annihilate bubbles in that portion. By placing the conductor Permalloy at different positions and by using a bipolar current pulse, a decoder line is achieved. In combining sets of such decoder lines, one can effectively select any one loop out of a number of loops.

(continued overleaf)

- c. Selective Steering Switch — This switch design is a modification of the existing single-level transfer switch. The input bubble stream has two alternative paths, depending on whether the transfer switch is active or not. Replacing the nonfunctional part of the Permalloy lead with a conductor lead completely avoids the Permalloy crossover problem. The transfer switch can be integrated into a selective annihilating decoder switch. Using the conductor lead as an inactive element, two complementary switch lines form a decoder line. Therefore control lines will be able to select storage loops.

Note:

Requests for further information may be directed to:

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Title to this invention has been waived under the provisions of the National Aeronautics and Space Act [42 U.S.C. 2457(f)], to the Rockwell International Corporation, 3370 Miraloma Avenue, Anaheim, California 92803.

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